A PLL BASED INDIRECT AUDIO FREQUENCY SYNTHESIZER

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By

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TO

My Father

C E R T I F I C A T E

This is to certify that the thesis entitled " A PLL Based Indirect Audio Frequency Synthesizer ", describes the work carried out by Mr Harshad B Shah under my supervision and that it has not been submitted elsewhere for a degree.

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Harshad Shah

ABSTRACT

An effort has been made to develop and fabricate a digitally programmable instrument having spot frequency generation and sweep generation capabilities with 3-digit accuracy in audio-frequency range. The basic block of such a system is a digitally programmable spot-frequency generation after which desired sweep can be obtained by external hardware. An indirect scheme using Phase-lock-loop (PLL) is taken up for this purpose and is developed in full detail. It uses four blocks for four frequency decades. The Hardware for such a system for two decades has been made using all commercially available components. The tests on the scheme shows that it has got frequency accuracy upto four digits and is capable of generating sweep-programmed by external hardware, for getting frequency response of any system or block. The feasibility of this system is thus established.

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CHAPTER 1

INTRODUCTION

There are two distinct approaches to the problem of frequency synthesis. One is to generate different fixed frequencies related to a reference frequency (usually a crystal reference), and the other is to generate a frequency sweep over a required range. Accuracy and stability of frequency are important criteria in the first case, whereas the main objective of the sweep generation is to obtain a specified range of frequencies swept in a prescribed (e.g. linear, logarithmic, etc) manner with time. Although most commercial sweep generators do provide for fixed frequency operation, the accuracy and stability of such a fixed frequency are generally considerably worse than those obtained with spot frequency synthesizers. However the advantages of both these approaches can be combined by designing a digitally programmable spot frequency synthesizer.

Jhaveri (1) has given a good account of various schemes for frequency synthesis. The schemes which are amenable to digital programming can be classified in two different categories

a) Direct frequency synthesis schemes

b) Indirect frequency synthesis using PLL

In the direct frequency synthesis schemes the required frequency increments are obtained from the accurate and stable

reference frequency by frequency multiplication, division and translation. A judicious mixture of these then give the desired output frequency. This output frequency will have the accuracy of the reference frequency, but this scheme involves high frequency filters and mixers having rather stringent requirements. On the other hand, indirect synthesis uses Phase Lock Loop (PLL), the Voltage Controlled Oscillator (VCO) of this PLL being made to oscillate with a frequency appropriately related to the reference frequency by using a digital frequency divider in the feedback path. This scheme suffers from short term stability, as like every practical closed-loop system, there is always some jitter on the output. The advantages of this scheme are simplicity and low-cost.

The objective of present project is to investigate the feasibility of using a PLL based indirect synthesis scheme for generating a stair-case audio-frequency sweep suitable for testing the frequency response of practical circuits. Agrawal (2) has designed a digital programmer, for use with frequency synthesizers, which provides four decades of frequency range, with a four digit setting for the frequency. Attempt is therefore made in the present project to design a compatible synthesizer, having four frequency ranges: 10 to 100 Hz, 100 to 1000 Hz, 1 to 10 KHz and 10 to 100 KHz.

In the next chapter the different concepts of indirect frequency synthesis are taken up and then a scheme capable of meeting our requirements is formulated, which is followed by the selection of design parameters to be used in implementing the scheme formulated and the complete block diagram of the system. In the third chapter the hardware realization of each block constituting the system is taken up one after another and actual circuits are given. The fourth chapter concludes the thesis with results and suggested modifications for further improvements.

CHAPTER 2

PROPOSED INDIRECT FREQUENCY SYNTHESIS SCHEME

In the first section of this chapter the principles of the basic PLL multiplier are discussed. In the next section the carrier concept in PLL is discussed. The third section is devoted to the formulation of the scheme capable of generating multi-decades of the frequencies, which is followed by discussion on selection of the design parameters. The chapter concludes with block schematic of complete system.

2.1. Basic PLL Frequency Multiplier

The schematic diagrame of a frequency multiplier using a PLL and a digital frequency divider is shown in Fig. 2.1.

When the loop is locked,

$$f_r = f_o/N$$

Where f_r is the reference frequency
f_o is the VCO output frequency
and N is the division ratio.

So the output frequency is a multiple of the reference frequency :

$$f_o = N f_r \qquad \text{------ (2.1)}$$

Now if we sweep the division ratio N, then at the output we get a sweep of frequencies as the reference frequency is being kept constant.

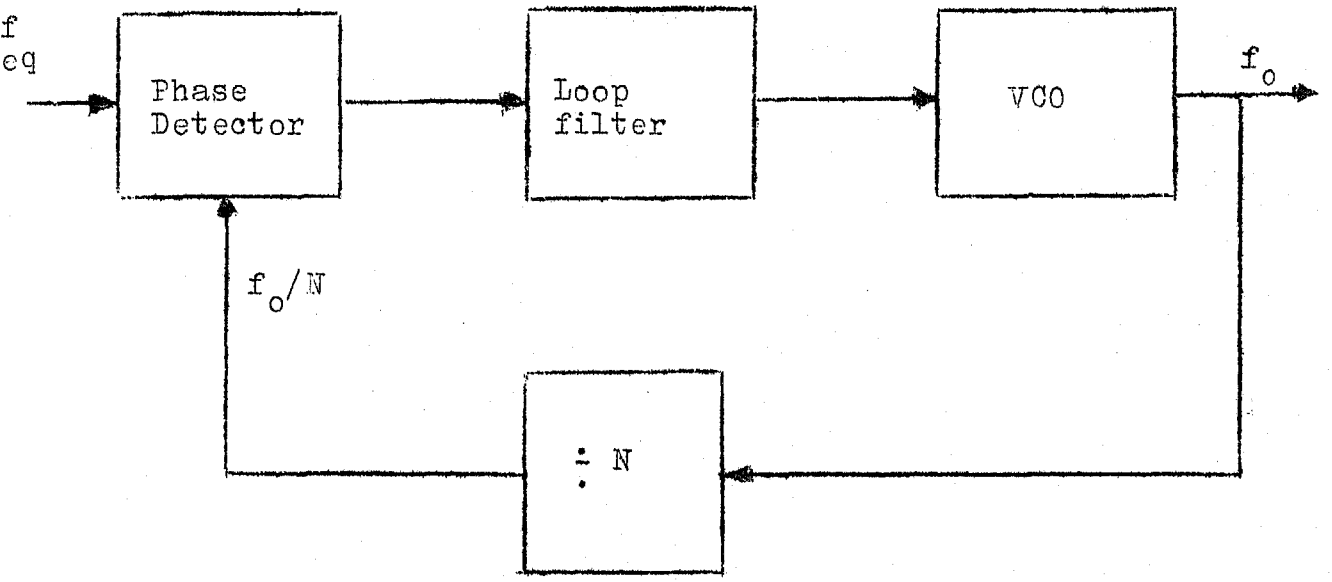


Fig. 2.1 Basic PLL

Let us now examine the possibilities of spurious locking, i.e, the possibility of the PLL to be locked without satisfying equ. 2.1. These possibilities arise out of the presence of harmonics in the Phase Detector (PD) inputs, as explained below.

Let the divider output contain the n^{th} harmonic (frequency - $n. f_o/N$) and the reference signal contain the m^{th} harmonic (frequency - $m.f_r$) such that the frequencies of these two harmonics are equal :

$$m. f_r = n. f_o/N$$

Clearly then, the PLL stays locked with an output frequency :

$$f_o = (m/n)\ N\ f_r \qquad \text{-------(2.2)}$$

So that, depending on values of m & n, the various possible values of f_o can result for same choice of N and f_r. Making the reference signal a sine wave leads to a considerable improvement in the situation as now $m = 1$ and eq. 2.2 reduces to

$$f_o = N\ f_r/n \qquad \text{------(2.3)}$$

This is usually referred to as harmonic locking and restricts the usable range of N. If the divider output is symmetrical square wave (N even) the minimum value of n is 3 (in a symmetrical square wave all even harmonics are absent) and as such a range of 1 : 2 for N is safely permissible. With such a restriction on N harmonic locking can be avoided by ensuring

that the lock range of PLL does not extend below the minimum frequency in the desired range.

2.2. Carrier Concept in PLL

From section 2.1, it is clear that we can not use a direct PLL for sweeping even one decade of frequency not to speak of the entire audio range. So the alternative is to use a carrier frequency during frequency synthesis and then to subtract it by mixing. Such a scheme is indicated in Fig. 2.2

N_o is number corresponding to the carrier frequency which means that $N_o f_r$ is our carrier frequency.

The division ratio is $N_o (1 \pm k)$; k being swept from k_1 to k_2 to generate frequency

$$f_o = N_o (1 \pm k) f_r \qquad \text{------(2.4)}$$

This output is mixed with the carrier frequency $N_o f_r$, and the lower side-band is selected by an Low-Pass Filter (LPF), so that we get our required band of frequencies as the final output :

$$F_o = f_o - N_o f_r = k N_o f_r \qquad \text{-----(2.5)}$$

In order to restrict the range of $N(= N_o (1 \pm k))$ to 1 : 2 , one has to ensure that :

$$1 + k_2 \leq 2 (1 - k_1)$$

or $$k_2 - 2k_1 \leq 1$$

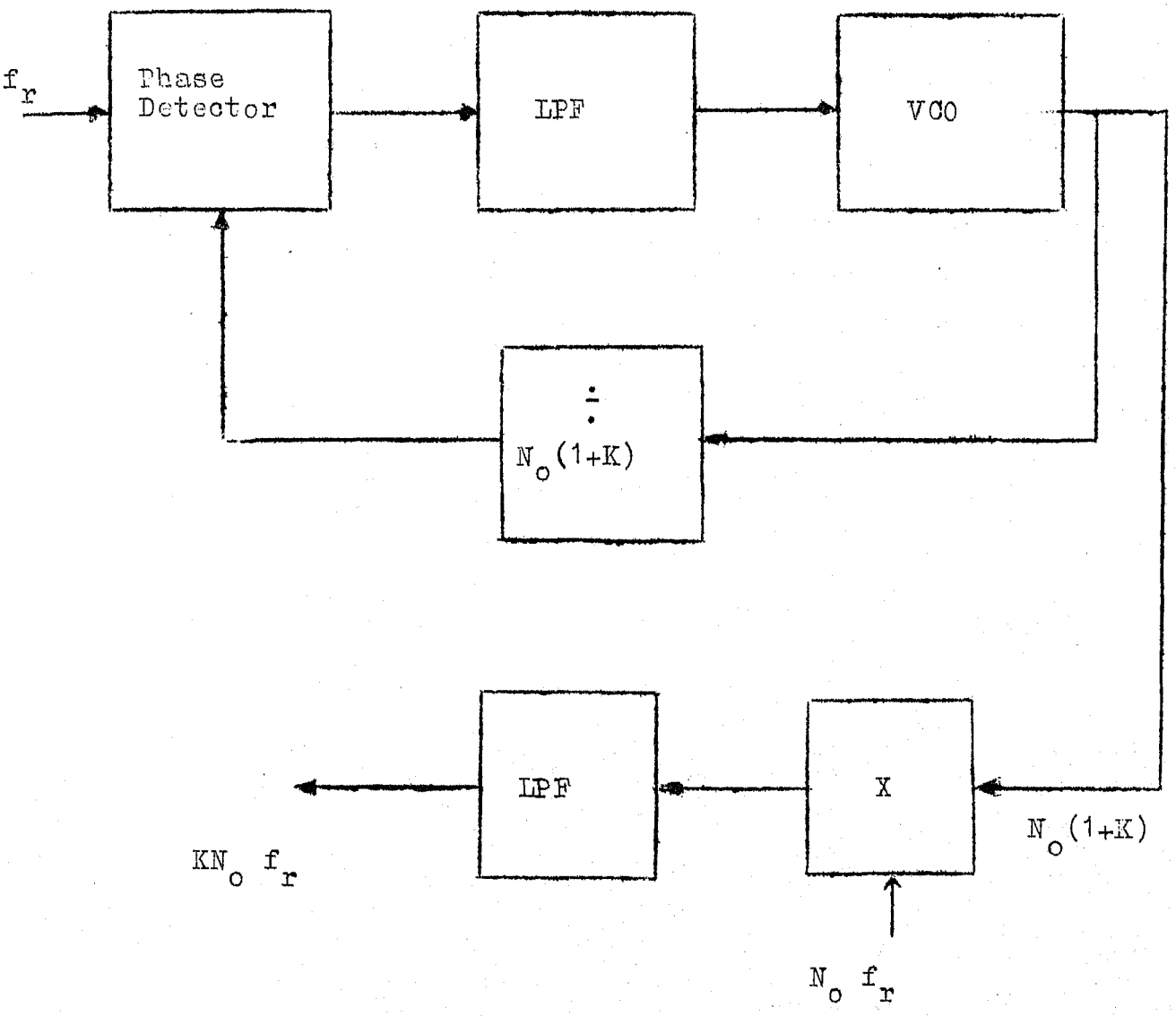


Fig. 2.2 Basic PLL with carrier

If no restriction is placed on the lower limit of k_1, then this requires

$$k_1 < k_2 \leqslant 1 \qquad \text{-----} (2.6)$$

Even with this restriction k_2/k_1 can be arbitrarily large in principle ; but as one has to use the same number of significant digits for setting the lower and upper limits of the frequency range, k_1 and k_2 have to have the same number of significant digits, say M clearly then

$$\frac{k_2}{k_1} \leqslant 10\ (1 - 10^{-M}) \qquad \text{-----} (2.7)$$

the equality being satisfied if a full decade is desired.

Multi-decade range cannot thus be achieved in this simple carrier scheme. One way to obtain more decades would be to use different PLL's for different decades. Such a scheme would, however, not be economically viable. Alternatively multiple decades of frequency can be achieved with a single PLL by using divide-and-mix scheme, as discussed in the following section.

2.3. Divide - and - Mix Scheme

The block schematic of this scheme is shown in Fig 2.3. Sweeping k from k_1 to k_2 results in a swept PLL output frequency $(1^{+} k)\ N_o\ f_r$; mixing this output with the carrier frequency $N_o\ f_r$ and selecting the lower side-band by an LPF gives the first decade $(k\ N_o\ f_r)$. The PLL output frequency is divided by 10 and mixed with $0.1\ N_o\ f_r$ to generate, after an LPF as before, the next lower decade $(0.1\ k\ N_o\ f_r)$. Successive decades can be

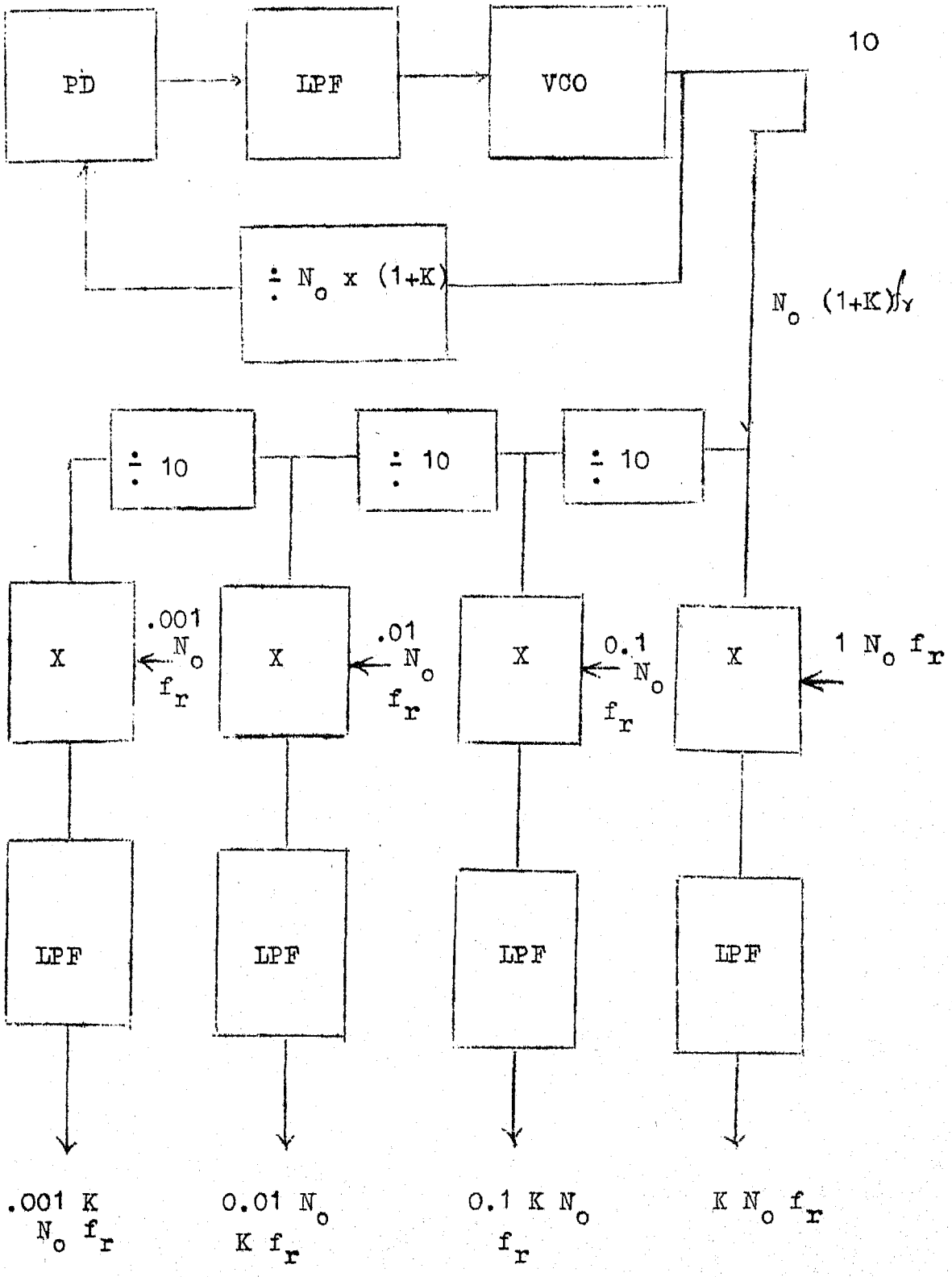


Fig. 2.3 Divide and mix scheme

obtained by further division of the PLL output frequency as well as the carrier frequency before mixing them together. The accuracy of the final output frequency remains the same as that of PLL output frequency in any decade.

2.4. Selection of the Design Parameters

The design parameters in the present divide-and-mix scheme are N_o , f_r, k_1, k_2 and M.

The maximum frequency in the instrument is 100 KHz. Hence carrier frequency should be at least double this to ease requirements of the LPF that follows the mixer to separate carrier from the signal.

A convenient choice for carrier frequency is therefore :

$$N_o f_r = 500 \text{ KHz} \qquad \text{-------(2.8)}$$

We have, from equs. 2.5 and 2.7

$$k_1 N_o f_r = 10 \text{ KHz} \qquad \text{------(2.9)}$$

$$k_2 N_o f_r = 100 (1 - 10^{-M}) \text{ KHz} \qquad \text{------(2.10)}$$

in view of the fact that the highest decade of frequencies commences from 10 KHz.

$$\therefore \quad k_1 = 0.02 \qquad \text{------(2.11)}$$

$$\text{and} \quad k_2 = 0.2 (1 - 10^{-M}) \qquad \text{------(2.12)}$$

The choice of the value of M depends on the jitter in PLL output frequency. As the reference frequency can be assumed to have stability of 1 part in 10^5, the PLL output frequency

also has the same long-term stability ; however, its short-term stability depends on LPF time constant, and an attempt to increase the stability by increasing the LPF time constant leads to a reduction in the capture range of the PLL. The short-term stability is thus an order of magnitude worse than the long-term stability. A 4-digit setting is therefore the maximum possible for N , leading to M = 3

Hence eq. 2.12 gives

$$k_2 = 0.1998 \qquad \text{------(2.13)}$$

and the only choice of N_o and f_r, compatible with eq. 2.8 are :

$$N_o = 5000 \qquad \text{-----(2.14)}$$

and $$f_r = 100 \text{ Hz} \qquad \text{-----(2.15)}$$

But if we use f_r as 100 Hz, the sweeping rate has to be low as the phase detector will be operating at 100 Hz. For this reason the carrier frequency, at which PLL works, should be as high as possible to make swoop rate faster. For this reason a boosted-up frequency sweep can be generated and then divided down to get the required basic sweep. So one can make the carrier frequency 5 MHz or 50 MHz instead of 500 KHz. The commercial PLLs are available for frequencies upto 35 MHz and hence carrier frequency is selected to be 5 MHz and now the sweep generated by PLL is 5.100 MHz to 5.999 MHz and then this can be divided by 10 to give us required basic sweep of 510.0 KHz to 599.9 KHz.

This results in f_r to be 1 KHz. But in view of having PD input to be symmetrical square wave, the prescaling by factor of 2 is needed to enable us to use flip-flop after chain of dividers (so that N is even for any setting of k). This results in value of f_r to be equal to 500 Hz which is adequate on speed considerations.

2.5 Complete Block Schematic of The Proposed Scheme

Fig 2.4 gives block schematic of the proposed scheme.

As discussed in previous paragraph, we need 500 Hz as the reference input of PLL. We also need 500 KHz, 50 KHz , 5 KHz and 500 Hz signals as the different inputs out of which one at a time is switched as the one input of the mixer. Hence the first block consists of Reference and Auxillary Frequency Generation in which we have crystal oscillator and chain of dividers. The next block in the system is different Band-Pass Filters (BPF) as all above signals have to be sine wave. So we have four different BPF for four different frequencies. The next block is PLL frequency multiplier. This consists of PLL which generates boosted-up sweep of 5.100 MHz to 5.999 MHz which is followed by divider to give us the basic sweep of frequencies. Then comes the mixer block, whose one input is carrier frequency or carrier frequency after successive division

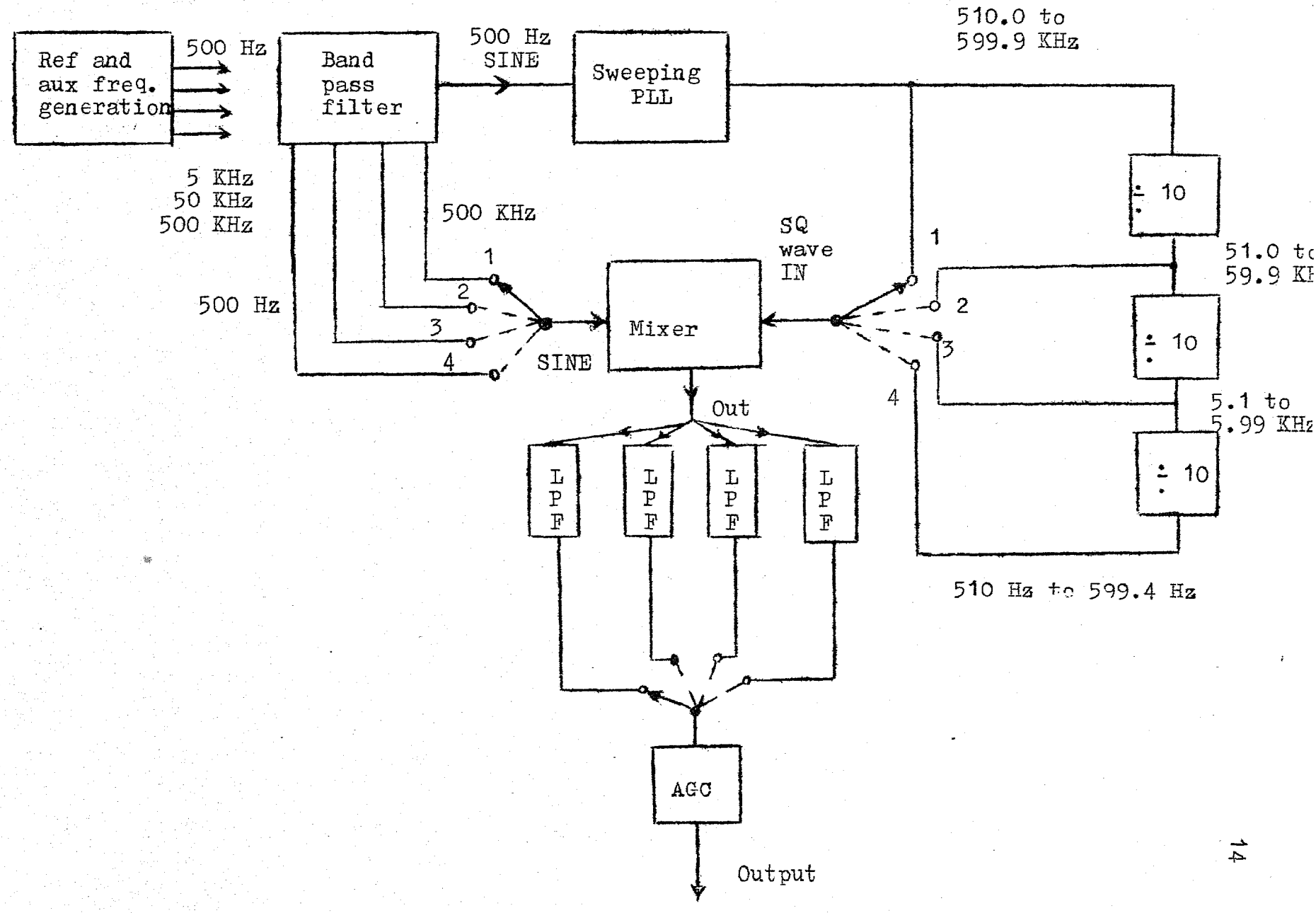


Fig. 2.4 Block diagram of the proposed scheme

(different sine wave frequencies outputed by different BPF) depending on range. The other input is also selected, from four different inputs, depending on range, these four inputs being the basic sweep and basic sweep after successive division by 10. This mixer gives us, the frequencies which are sum of two input frequencies of the mixer, difference of two input frequencies, sum of different harmonics of the input frequencies and difference of different harmonics of the input frequencies as the output. The next block is bank of Low Pass Filters (LPF). The cutput of the mixer goes to the inputs of four different LPF. These low pass filters select the correct frequency of interest from the mixer output, i.e. the difference of the two input frequencies of the mixer. The output of these LPF is switched (again depending on range) to the input of the Automatic Gain Control (AGC) circuit which is the last block of the system. This AGC stabilizes the amplitude to the same value for different output frequencies such that we get constant amplitude output signal for practically all frequencies of interest.

CHAPTER 3

HARDWARE REALIZATION

This chapter deals with actual hardware realization of the blocks constituting the system.

3.1 Reference and Auxillary Frequency Generation

In realizing any reference oscillator the main criteria are frequency accuracy and frequency stability with time, temperature and components change. For these reasons a master crystal oscillator of 10 MHz frequency is selected and then reference frequency and all other auxillary frequencies (500 KHz, 50 KHz, 5 KHz) are obtained by putting a chain of dividers from the master clock.

Fig 3.1 shows the master crystal oscillator. It uses standard TTL NOR (SN 7402) gates and a 10 MHz crystal to give us 10 MHz Master reference frequency. Standard astable configuration is used for this purpose. Resistors R_1 and R_2 keep gates at their proper threshold values. The capacitor trimmer C_T gives fine variations in frequency.

The auxillary frequency sources required are 500 KHz, 50 KHz, 5 KHz and 500 Hz.

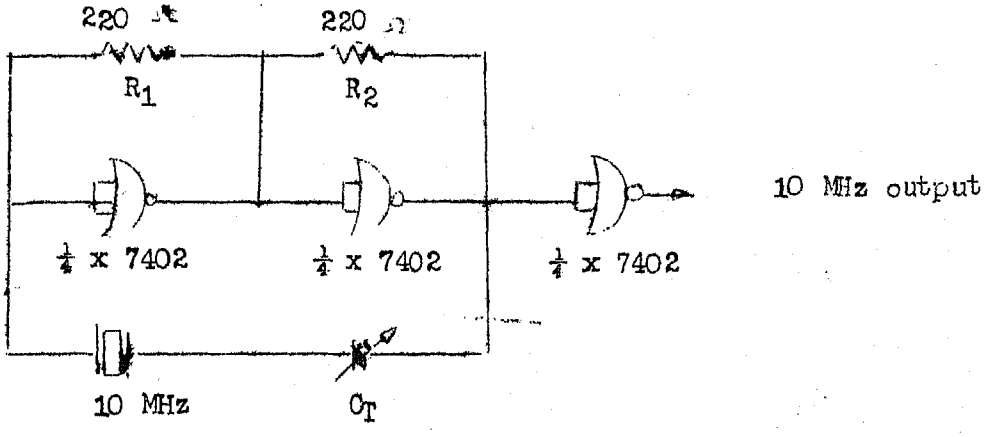


Fig. 3.1 - Master Crystal Oscillator

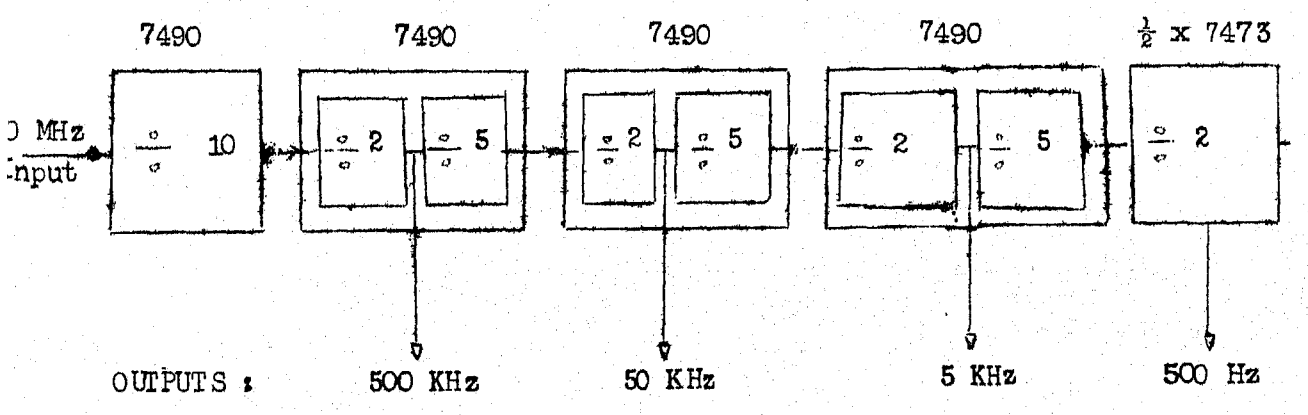


Fig. 3.2 - Chain of dividers.

All these frequencies can be directly generated from 10 MHz master reference frequency by putting chain of dividers as shown in Fig 3.2.

3.2. Band Pass Filters (BPF)

We need four different BPF to convert 500 KHz, 50 KHz, 5 KHz and 500 Hz TTL signal to sine wave. All of these signals are required to go as one of the input of mixer for different ranges. 500 Hz sine wave is also required to go as PLL reference input.

The specifications of these filters will be, that, it should attenuate third harmonic frequencies which are present in TTL output. The design of these filters is simple as there is wide separation between pass-band and stop-band frequencies of the mixer.

For 500 KHz filter, as the pass-band frequencies are near to standard Intermediate Frequency (I.F.) used in AM Radio-receivers, an Intermediate Frequency Transformer (IFT) is used which follows the passive R-C low-pass filter, to give us reasonably good sine wave. Fig 3.3. gives circuit diagram for this case.

For other band-pass filters a passive low-pass followed by second order active Voltage Controlled Voltage Source (VCVS) band pass filter is used.

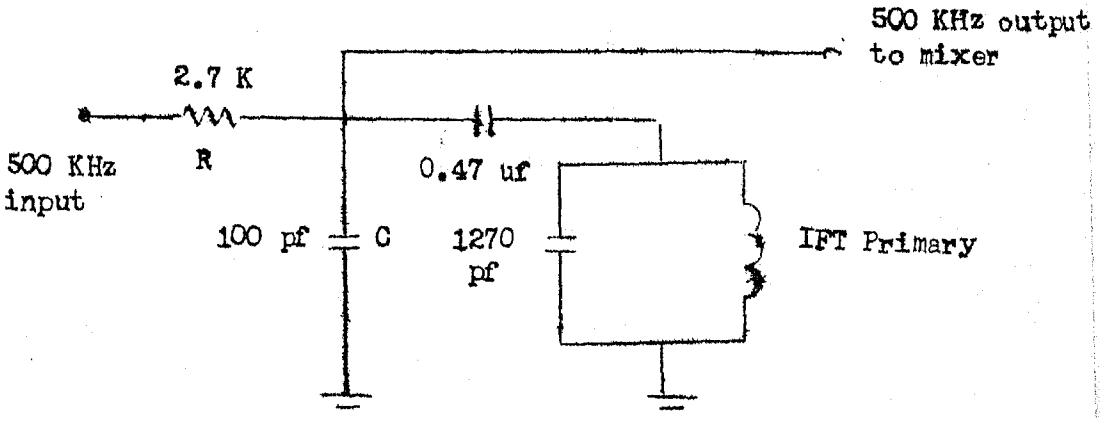
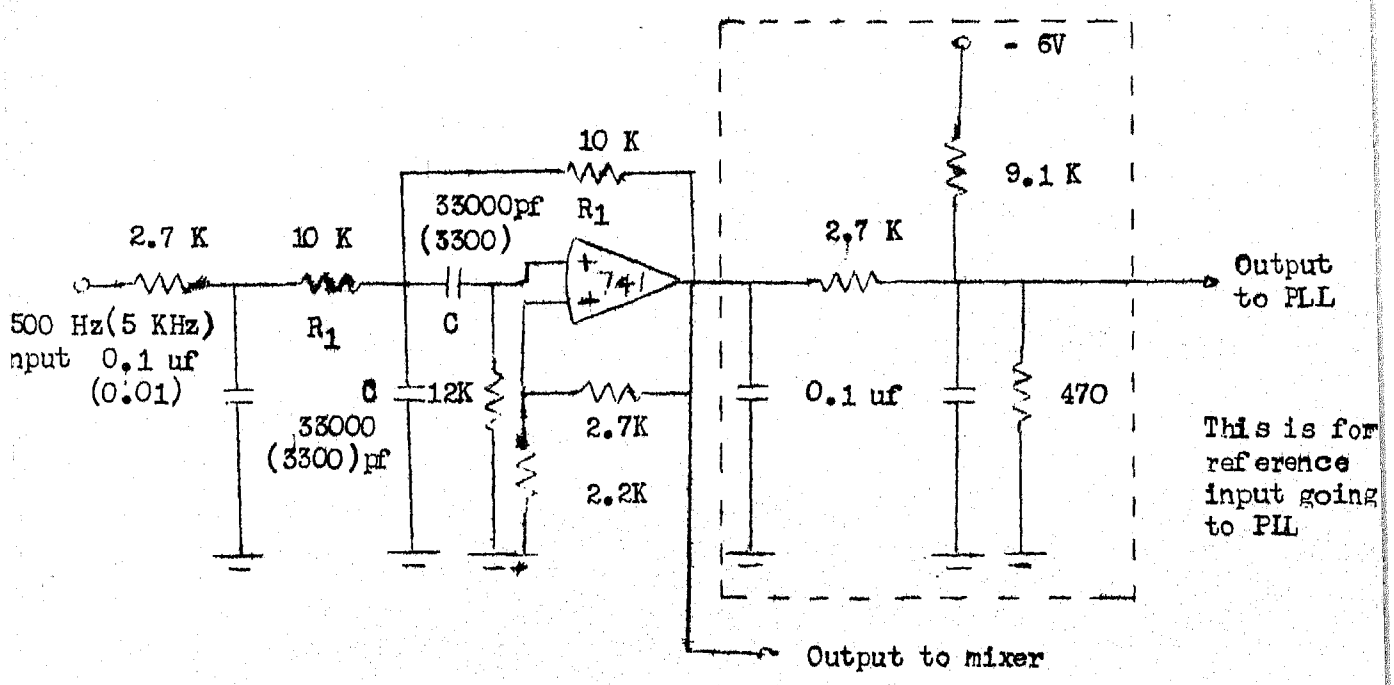


Fig. 3.3 500 KHz Band Pass Filter



Values in brackets are for 5.00 KHz filter.

Fig. 3.4 500 Hz and 5.00 KHz Band Pass Filters

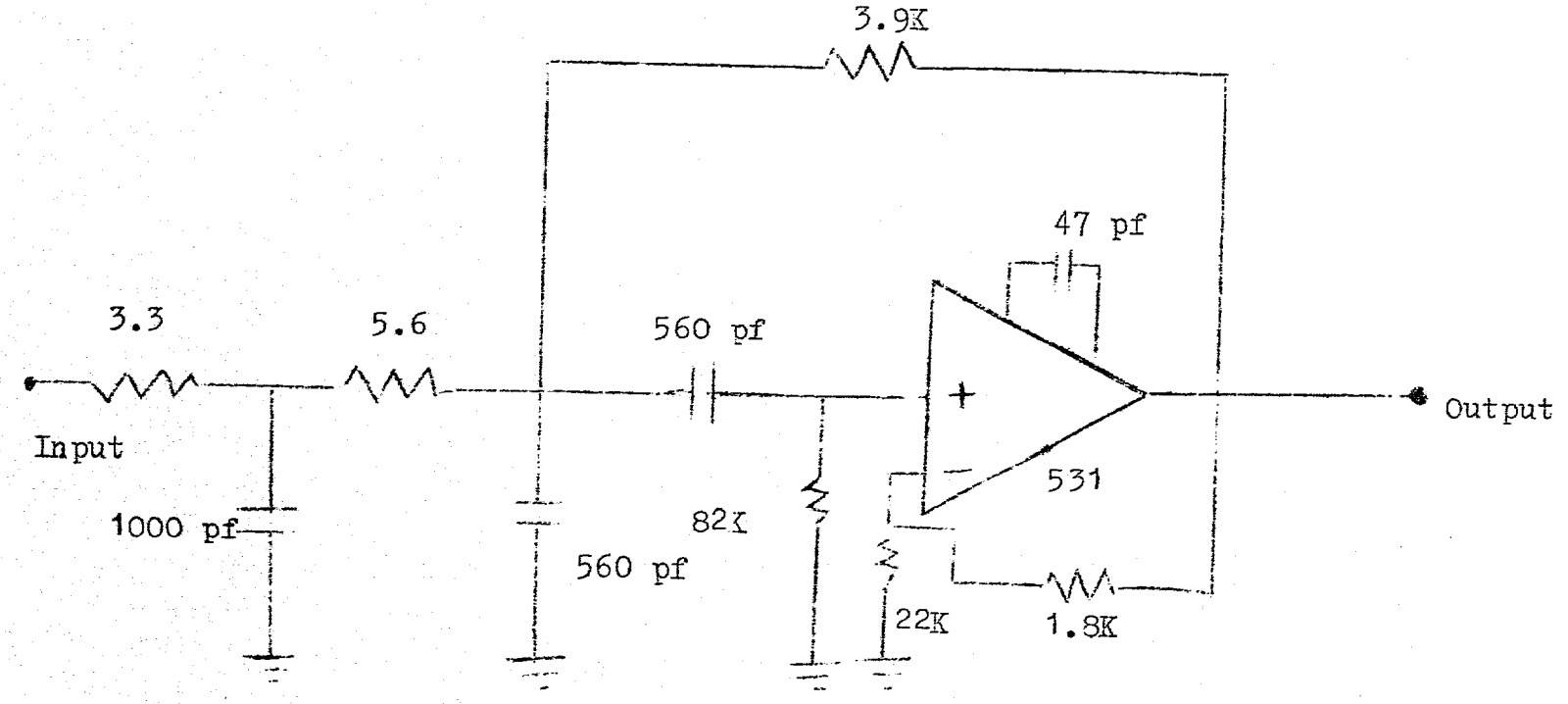


Fig. 3.5 50 KHz filter

The complete circuit diagrams for 50 KHz, 5 KHz and 500 Hz filters are given in Fig. 3.4 and Fig. 3.5.

The passive low-pass filter has get cut-off frequency :

$$f_c = \frac{1}{2\pi RC} \qquad \text{-------(3.1)}$$

which is selected near centre frequency of BPF (slightly on higher side). For VCVS band pass filters the center frequency is given by :

$$f_c = \frac{\sqrt{2}}{2\pi R_1 C} \qquad \text{------(3.2)}$$

Even though active filters give low Q, a reasonably good performance can be expected from them because of the facts that stop-band frequencies are three times the pass-band frequencies and the stop-band frequencies are already attenuated by passive low-pass filters.

The PLL restricts the input reference frequency amplitude and it requires some dc level. For these reasons an attenuator and level shifter is used with 500 Hz filter which is shown in dotted line block in Fig - 3.4.

3.3. The PLL Frequency Multiplier

Fig 3.6 gives detailed circuit diagram for this block which uses a highly sophisticated monolithic PLL (XR-215), Schmitt trigger (7413), four cascaded programmable divider (74190) in down counting mode, the most significant digit counter of which have

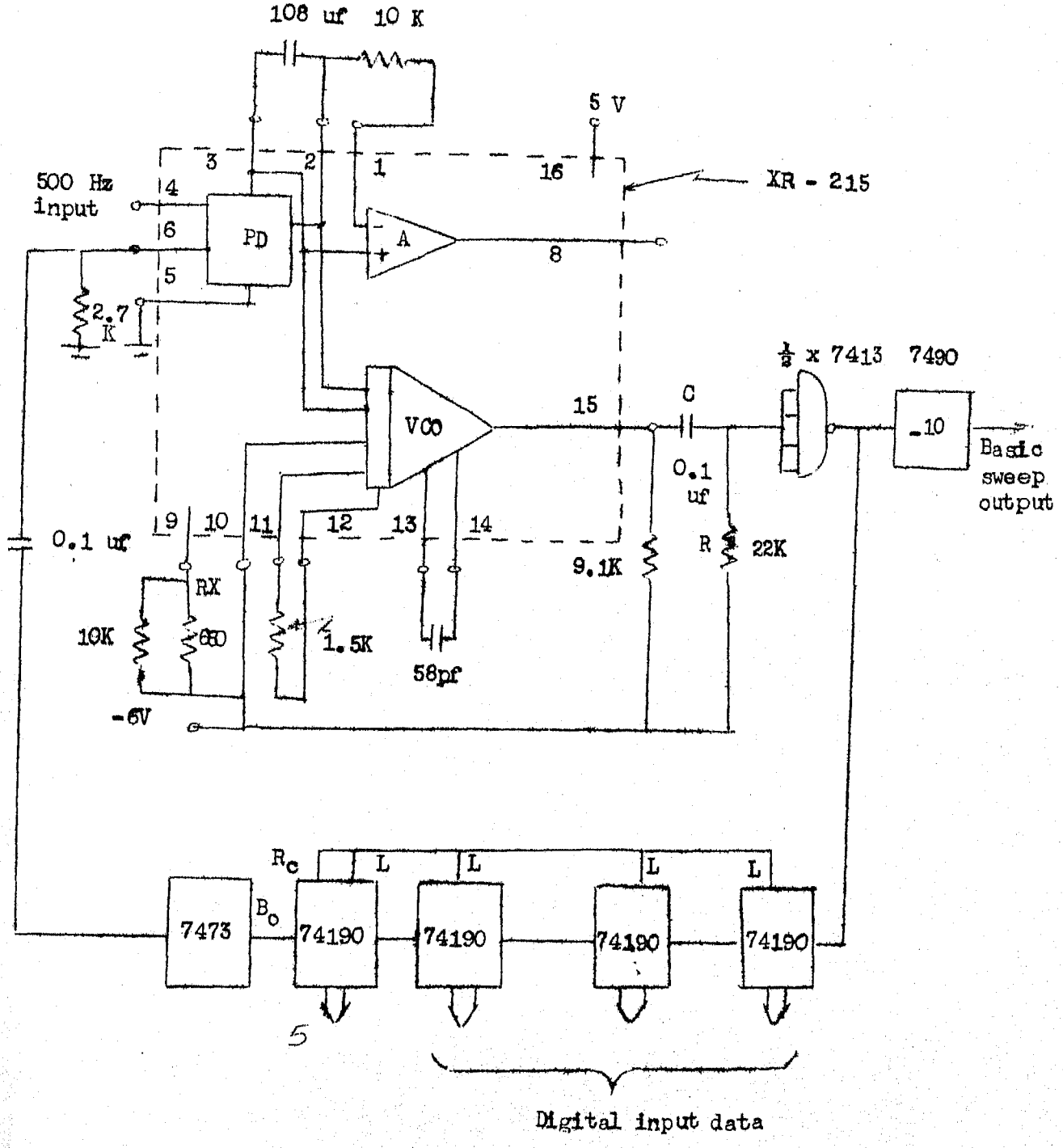


Fig. 3.6 - The PLL frequency multiplier

permanent data-in as 5 (corresponding to carrier frequency), while the remaining three digit dividers take input data, which varies from 100 to 999 depending on frequency to be generated, a flip-flop (7473) which is used to make output of this chain, a symmetrical square wave.

The VCO free-running frequency for PLL XR-215 is given by following equation :

$$f_o = \frac{200}{C_o} \qquad \text{-------(3.3)}$$

where f_o is VCO output frequency and C_o is VCO timing capacitor in uf.

The timing capacitor C_o is to be connected between pin 13 & 14.

The free-running frequency can be increased by connecting an external resistor R_x between pins and 10 of XR-215. Now the output frequency is given by

$$f_o = \frac{200}{C_o} \left(1 + \frac{0.6}{R_x}\right) \qquad \text{-----(3.4)}$$

R_x is in Kiloohms.

The 10 K Ohm preset potentiometer in parallel with 680 Ohm resistor is used for trimming the free-running frequency.

The low-pass filter is formed by putting a capacitor between pins 2 and 3. This capacitor should be as high as possible to have minimum jitter in the output. The capture range puts the upper limit on this capacitor as higher the capacitor value small is the capture range. In the present case the PLL has to have lock

when division ratio changes from 2 x 5999 to 2 x 5100, in other words PLL should be able to capture at division ratio 2 x 5100 and should be able to maintain the lock upto at least 2 x 5999. The resistor R & C is used to make PLL output, a TTL compatible for schmitt trigger input.

Three digit BCD lines are brought out for either manual control or remote control of the instrument to use this spot frequency generator for sweep generation.

3.4. The Mixer

The mixer's two inputs are, 500 KHz and basis sweep (510.0 KHz to 599.9 KHz) for the first decade, 50 KHz and sweep signal which is now 51.00 KHz to 59.99 KHz and so on for successive lower decades. Our aim is to find difference of these two inputs after passing the output of this mixer from appropriate filter, a low-pass in present situation.

One would like to use square waves for both the inputs of this mixer as it results in less hardware.

Analysing this mixer's output content (for first decade) if both the inputs are made square wave.

The output of the mixer will be of the form

$$f_o = L f_c \pm M f_s \qquad \text{----(3.5)}$$

Where f_s = 500 KHz

f_c = Sweep ranging from 510.0 to 599.9 KHz

Let f_c = 510.0 KHz

and L & M are integers corresponding to the harmonics of input.

Table 3.1 : Harmonic Analysis of Mixer Output

L \ M	1	2	3
1	10 K 1010 K	490 K 1510 K	990 K 2010 K
2	520 K 1520 K	20 K 2020 K	480 K 2520 K
3	1030 K 2030 K	530 K 2530 K	30 K 3030 K

From the above table we can see that when L and M are same their difference, i.e. difference of same harmonics of input signals, will also fall in pass-band (which is 100 KHz for present (first decade) situation) of the low-pass filter which follows this mixer. So as a result of this analysis it can be concluded that one cannot use both inputs of the mixer as square wave. This problem can be eliminated by using only one input as sine wave.

As one input of this mixer is constant frequency (for particular range selected) and other is sweep, the constant frequency input signal is made sine by using band-pass filters, the design of which has been discussed in Section 3.2.

For the purpose of this mixer, double balanced modulator demodulator (LM 1496) chip which produces product of an inpur (signal) voltage and a switching (carrier signal).

Fig. 3.7 gives schematic circuitdiagram of this integrated circuit chip.

A resister to ground from bias terminal fixes the bias constant current source current which is same for Q_7 and Q_8 also. This current depends on the negative supply voltage and value of resistor connected to the bias terminal. Same current will pass from Q_5 and Q_6 when there is no signal. At gain adjust pins which are emitters of two transistors a resistor is connected to direct current from one transistor to another according to signal. Total current remains same which is equal to $2.I_{c9}$.

The current in Q_5 and Q_6 is modulated by signal input. At one stage currents can be $I_{c9} + I_s$ and $I_{c9} - I_s$ where I_{c9} is bias current and I_s is signal current.

Transistors Q_1 , Q_2 , Q_3 , Q_4 which makes a differential pair are used in switching mode which are switched with carrier (switching) signal. At any stage either transistors Q_1 and Q_4 an "ON" or Q_2 & Q_3 are "ON".

And so at output (Resistors from output to V_{cc} are to be connected-they-being open-collector type) we get product of two signals.

To separate required component from output, this output has to be passed from appropriate filters. In the present case

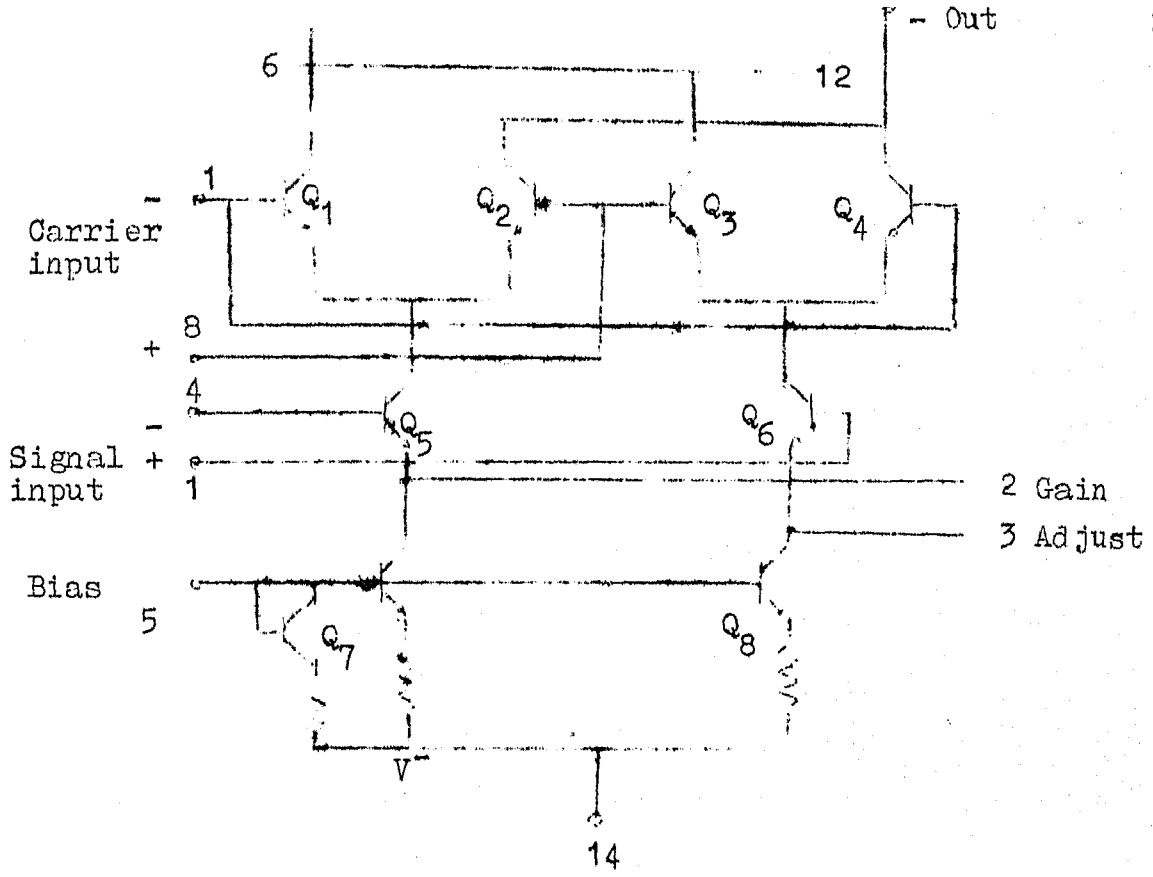


Fig. 3.7 Schematic diagram of I.C. 1496

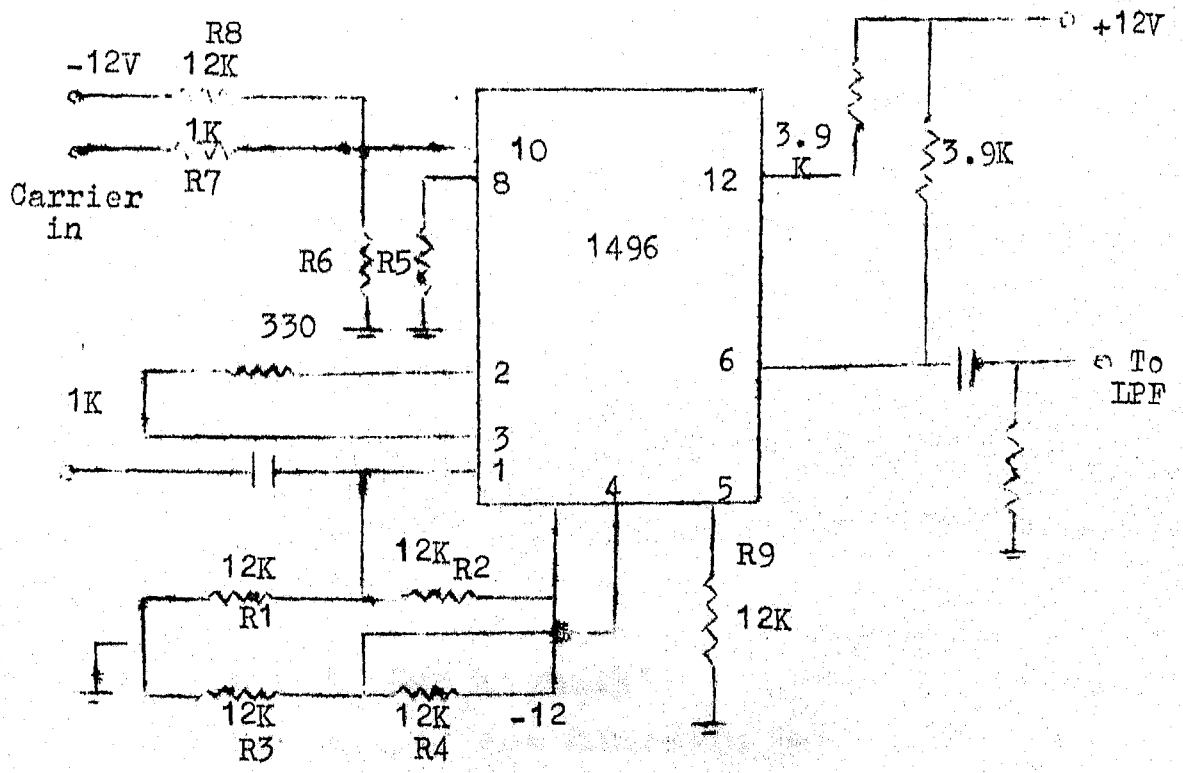


Fig. 3.8 The Mixer

the required band is upto 100 KHz. So the output is passed from a 100 KHz low-pass filter to give us required output.

Also while using this I.C. it is necessary to bias signal port negetively with respect to carrier port. Fig. 3.8 gives complete circuit diagram of this mixer. Resistors R_1 , R_2 , R_3, R_4 biases pin 1 and 4 (signal port inputs) to half the negetive bias. Carrier port (pins 8 and 10) is directly grounded via resistor R_5 and R_6. R_6 , R_7 , R_8 also works as level shifter, to make carrier signal suitable for LM 1496. R_9 is used to adjust the bias and R_{10} and R_{11} works as collector loads for the outputs.

The output is ac coupled via capacitor to the input of the filters.

3.5. Low Pass Filters (LPF)

The function of these low-pass filters is to extract required frequency components from the mixer output. Four different filters one for every range are used for this purpose. Fig. 3.9. and Fig. 3.10 gives circuit diagram for 100 K LPF and 10 K LPF respectively. The values in the brackets are for 100 Hz and 10 Hz filters.

All the filters are made fourth order VCVS type active low-pass filters. The exhaustive analysis and design procedure can be had from Hilburn & Johnson (3).

3.6. Automatic Gain Control (AGC)

The outputs of above filters will have varying amplitude

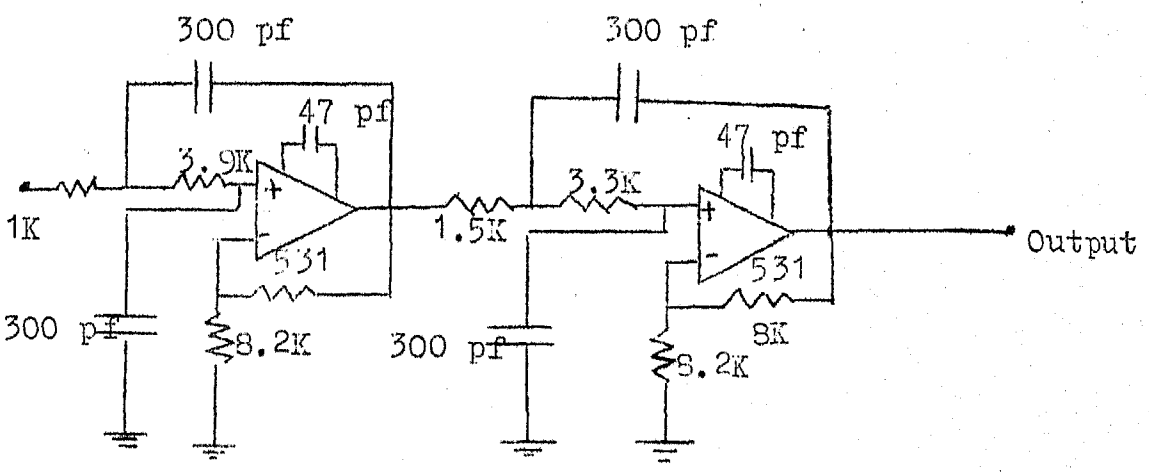
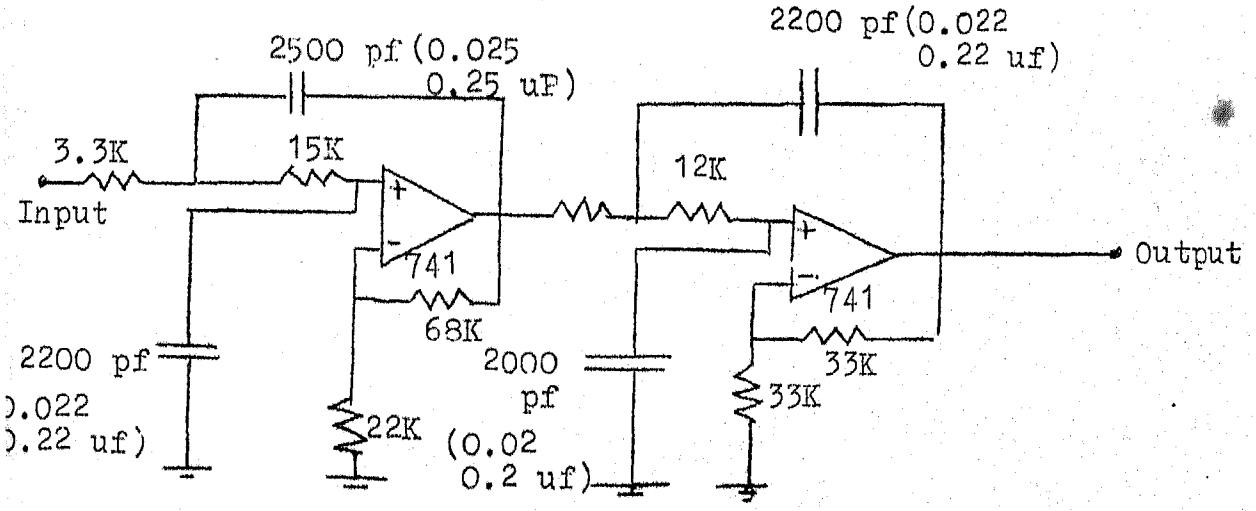


Fig. 3.9 100 KHz LPF



(values in paranthesis are fof 1 KHz and 100 KHz LPF respectively.)

Fig. 3.10 10 KHz LPF

as one can not make flat pass-band filter - as gain can not be made constant over a complete pass band of filter. All the filters are to be followed by AGC circuit.

The circuit diagram of AGC is given in Fig. 3.11. The function of this circuit is simple. The FET (BFW 10) is used as Voltage Variable Resistor(VVR) and this is used as one of the gain controlling resistor of amplifier. This amplifier is followed by precision rectifier.

Appropriate dc is injected in this stage so that output of this rectifier can be directly fed to the gate of FET after filtering.

Now if amplitude of output increases, the negative bias on the gate of FET also increases, which results in increase in effective resistance offered by FET which in turn reduces the gain of amplifier and vice-versa.

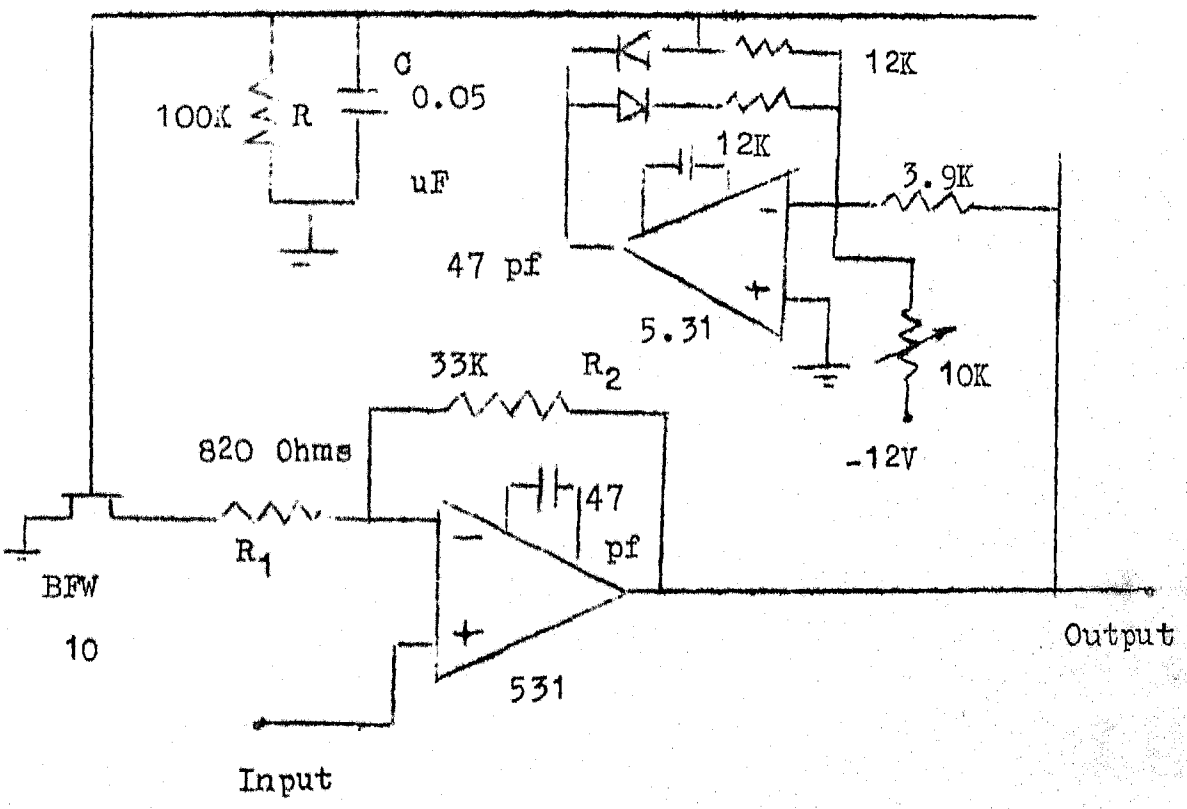


Fig. 3.11 Automatic Gain control circuit

Chapter 4

RESULTS AND CONCLUSIONS

The hardware developed in Chapter three is actually fabricated and tested for first two decades. The following table shows the frequency setting, the output frequency and its variations with time, for few spot frequencies.

Table 4.1 : Frequency Setting Vs. Frequency Output

Freq. setting	Output frequency after it has settled	Output frequency variations immediately after setting	Output frequency variation after 10 sec.	Output freq. variation after 1 minute
2.57 KHz	2.569 KHz	2.1 KHz - 2.9 KHz	2.52 KHz - 2.60 KHz	2.568 KHz - 2.571 KHz
25.9 KHz	25.87 KHz	25.3 KHz - 26.2 KHz	25.8 KHz - 26.0 KHz	25.86 KHz - 25.88 KHz
4.05 KHz	4.049 KHz	3.6 KHz - 4.3 KHz	3.96 KHz to 4.08 KHz	4.047 KHz - 4.051 KHz
40.7 KHz	40.68 KHz	40.2 KHz - 41.1 KHz	40.60 KHz to 40.74 KHz	40.67 KHz - 40.69 KHz

From the table we can see that the variation in output frequency immediately after the setting of the frequency is large. This can be expected as the reference frequency at which PLL works is 500 Hz. So short-term instability according to this frequency will be there. Also the low-pass time constant is

approximately 0.6 seconds. settling time is also proportional to this. Higher the LPF time constant (LPF - capacitor), the capture range is smaller and thus output frequency will have better stability, hence one would like to have as high value of this capacitor as possible. On other hand higher the time constant, larger is the time taken for settling. So there is trade-off between speed of sweeping and stability of frequencies, in selecting this time constant. If one can afford slower sweep then he can have higher stability in this system.

As we go on increasing sweep rate, after some time, the output frequency will start lagging behind the setted frequency and if still the sweep rate is increased, the PLL will fail to maintain lock. The maximum sweep rate without any lagging and with lagging are given

Maximum sweep rate without any lagging	-65 Hz
Maximum sweep rate with some lagging	-450 Hz

Which means that if we increase sweep rate beyond 18 KHz, the PLL will fail to maintain lock.

Suggested Modifications

In the present system, even if we can afford slower sweep rate the capture range can not be increased beyond some point, because PLL will loose lock.

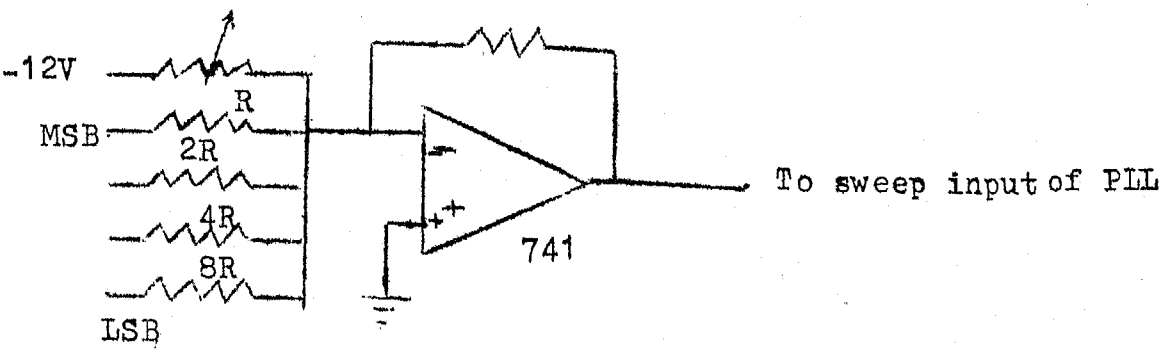


Fig. 4.1 Tracking PLL

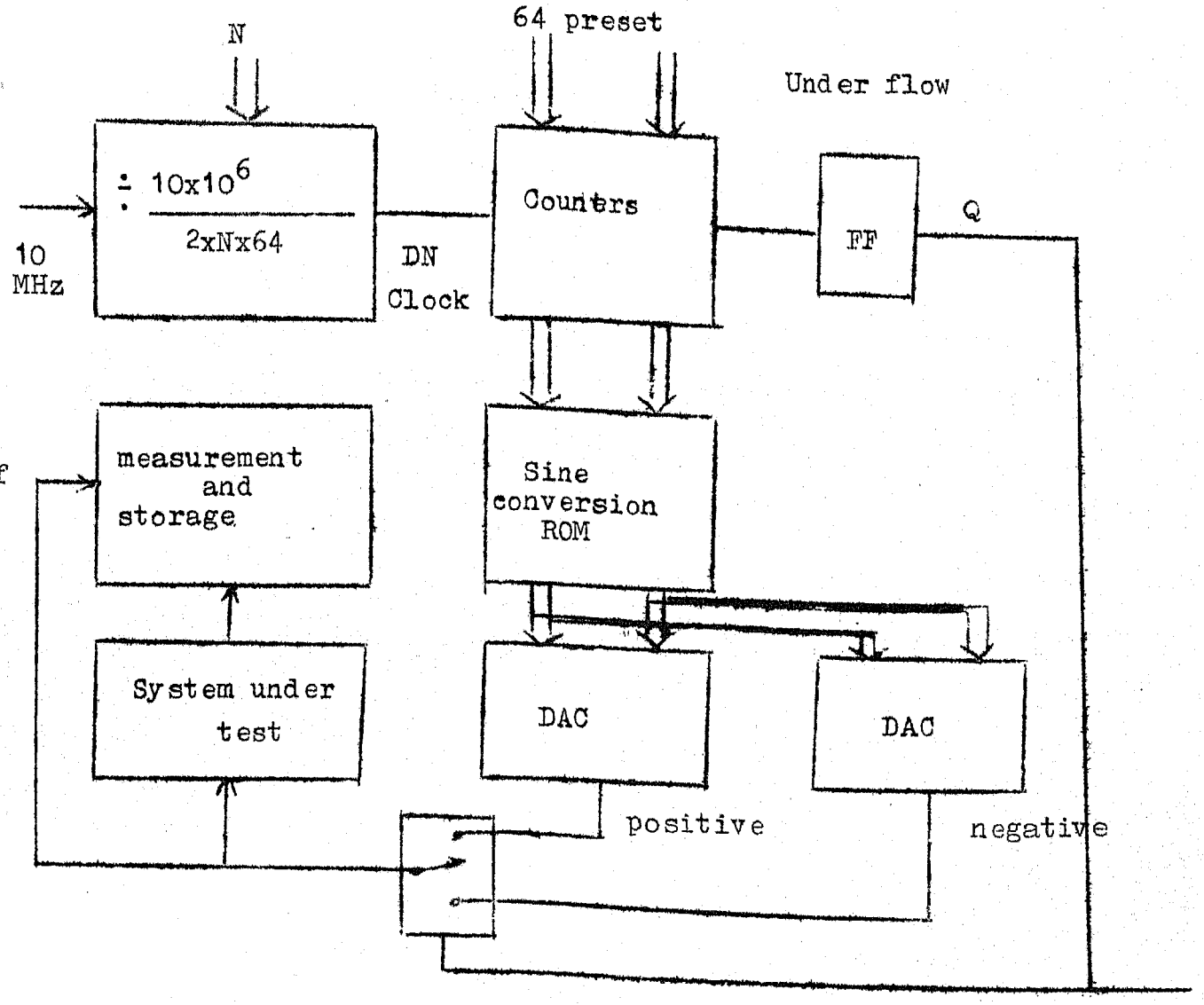


Fig. 4.2 Alternate low frequency synthesizer

For this problem one can use tracking PLL in which VCO frequency tracks the frequency at which it is asked to lock. The PLL XR-215 being highly sophisticated PLL gives facility of sweeping VCO frequency by giving negative bias at sweep input. Fig. 4.1 gives a scheme for such a tracking PLL. It uses a four bit digital-to-analog converter which takes, the four most significant bits of the digital input to PLL, as input of it and with appropriate DC injected at its input, gives the output which can be feed to sweep input of PLL. Thus with the change in the division ratio (most significant digit) the VCO frequency also changes. Now with this tracking PLL one can make PLL very "tight" as the capture range required is very low and so LPF time constant can be increased. Although this scheme gives some problems they can be overcome .

Also this scheme is prone to more jitter in lower decades especially in 10 Hz to 100 Hz decades. For this reason the alternative way to generate this decade and lower decades (if desired) is as follows. The schematic is given in Fig. 4.2.

The frequency F, required to be generated (frequency less than 100 Hz) is fed to the logic circuit which calculates

$$X = \frac{10 \times 10^6}{2 \times F \times 64} \qquad (4.1)$$

where F is frequency to be generated.

Now 10 MHz clock is divided by this number X. The output of this gives 64 clock pulses in the 180° of the frequency to be generated. This output goes to the input of the programmable counter, which is resetted when it reaches to 64, at this instant a flip-flop is also toggled. The output of this counter goes to the sine conversion ROM, which generates 8-bit digital data which is digitally equal to the sine of the input (i,e. output is digitally equal to $\sin(\frac{180}{64} \times \text{Address})$. This output is fed to two DAC, one generates a positive cycle and another a negative cycle. An analog multiplexer selects one out of two alternatively at each 180° (the signal for this is given by flip-flop). The multiplexer gives the required output.

Hence the combination of these two schemes, the present scheme and the above suggested scheme can give us frequency synthesizer for any range. As the suggested scheme can give us any frequency which is less than 100 Hz, even 0.01 Hz, while the PLL synthesizer works satisfactor above 100 Hz, The combination eliminates all the problems, which this instrument is prove to at lower frequencies.

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